9. The method of claim 7, wherein the removing the first preliminary mask pattern structure includes removing the first sacrificial pattern.

10. The method of claim 9, wherein the forming the second mask pattern structure includes removing the fourth sacrificial pattern.

11. The method of claim 9, wherein the forming the second pattern structure includes removing the third sacrificial pattern.

12. A method of forming patterns of a semiconductor device, the method comprising:

forming first and second hard mask layers, the first hard mask layer formed on an etch target layer, the etch target layer having first and second regions, and the second hard mask layer formed on the first hard mask layer;

forming a first preliminary mask pattern and a first spacer on the second hard mask layer on the first region, the first spacer being on a sidewall of the first preliminary mask pattern;

forming second and third preliminary mask patterns on the second hard mask layer, the second preliminary mask pattern formed on the second region and having an upper surface substantially coplanar with an upper surface of the first preliminary mask pattern, the third preliminary mask pattern formed on the second preliminary mask pattern, and the third preliminary mask pattern having an etching selectivity with respect to the first preliminary mask pattern,

forming a second spacer on sidewalls of the second and third preliminary mask patterns;

removing the first preliminary mask pattern;

forming first and second mask pattern structures by partially removing the second hard mask layer using the first and second spacers and the second and third preliminary mask patterns as an etching mask, the first mask pattern structure formed on the first region and having a first width, the second mask pattern formed on the second region and having a second width, the second width being greater than the first width;

forming third and fourth spacers on sidewalls of the first and second mask pattern structures, respectively;

forming third and fourth mask pattern structures by partially removing the first hard mask layer using the third and fourth spacers and the first and second mask pattern structures as an etching mask, the third mask pattern structure formed on the first region and having a first upper surface, the fourth mask pattern structure formed on the second region and having a second upper surface, a height of the second upper surface being greater than a height of the first upper surface; and

forming first and second patterns by partially removing the etch target layer using the third and fourth mask pattern structures as an etching mask, the first pattern formed on the first region and having a third width, and the second pattern formed on the second region and having a fourth width, the fourth width being greater than the third width.

13. The method of claim 12, wherein

the forming the second mask pattern structure further includes removing the third preliminary mask pattern; and

the forming the fourth mask pattern structure further includes removing the second preliminary mask pattern.

14. The method of claim 12, wherein

the forming the first mask pattern structure further includes removing the first spacer; and

the second mask pattern structure is formed such that at least a first part of the second spacer remains.

15. The method of claim 12, wherein

the forming the first spacer includes,

forming the first preliminary mask pattern on the second hard mask layer,

forming a spacer layer on the (i) second hard mask layer and (ii) the first preliminary mask pattern,

forming a mask layer on the spacer layer on the second region, and

partially removing the spacer layer formed on the first region to form the first spacer; and

the forming the second spacer includes,

forming the second preliminary mask pattern on the second hard mask layer,

forming the spacer layer on the (i) second hard mask layer and (ii) the second preliminary mask patterns,

forming the mask layer on the spacer layer on the second region;

removing the mask layer, and

partially removing the spacer layer on the second region to form the second spacer.

16. A method of forming patterns of a semiconductor device, the method comprising:

forming a height difference between a first preliminary mask pattern on a first region of a layer structure and a second preliminary mask pattern on a second region of the layer structure by etching at least a portion of the first preliminary mask pattern and at least a portion of the second preliminary mask pattern, the layer structure including a plurality of mask layers stacked on an etch target layer, the etch target layer on a substrate; and

forming a first pattern structure on the first region and a second pattern structure on the second region by etching the plurality of mask layers, the etching of the plurality of mask layers controlled to maintain the height difference while forming of the first pattern structure and the second pattern structure.

17. The method of claim 16, wherein

the first preliminary mask pattern includes a first sacrificial pattern on a second sacrificial pattern; and

the forming the height difference includes,

forming a spacer layer on an upper surface of the first sacrificial layer, on a sidewall of the first preliminary mask pattern, on an upper surface and on a sidewall of the second preliminary mask pattern,

etching at least a portion of the spacer layer on the upper surface of the first preliminary mask pattern, and

creating the height difference by removing the first sacrificial layer and the portion of the spacer layer from the upper surface of the second preliminary mask pattern.

18. The method of claim 17, wherein

the etching at least a portion of the spacer layer on the upper surface of the first preliminary mask pattern forms a first spacer on the sidewall of the first preliminary mask pattern; and